

CLAIMS

What is claimed is:

1. A method for designing an integrated circuit, comprising:
receiving data specifying a plurality of interconnects and components of a design
of an integrated circuit; and
optimizing the design of the integrated circuit, wherein data specifying the
plurality of interconnects and devices of the integrated circuit is
optimized based on at least one of bandwidth, latency, scalability, and
isochronous interconnect configuration.
2. The method as described in claim 1, wherein the optimized data is programmed
into a self-programmable integrated circuit so as to provide the designed
integrated circuit.
3. The method as described in claim 1, wherein the optimized data is utilized to
synthesize an integrated circuit having the specified design.
4. The method as described in claim 1, wherein the optimized design includes a
specified characteristic for the interconnect, wherein the specified characteristic
includes at least one of bandwidth, latency and scalability.
5. The method as described in claim 1, wherein a direct connectivity definition,
derived the optimized data, is utilized to synthesize an integrated circuit.
6. The method as described in claim 1, wherein optimizing includes at least one of
arranging components of the integrated circuit and specifying bandwidth
between components.

7. The method as described in claim 1, wherein optimizing is performed without user intervention by an agent.
8. The method as described in claim 1, wherein the integrated circuit is at least one of an application specific integrated circuit (ASIC) and multiple application specific integrated circuits (ASICs).
9. The method as described in claim 1, wherein interconnects not specified by a user are automatically configured by an agent.

10. A self-programmable integrated circuit, comprising:
 - a processor suitable for performing a program of instructions, the processor accessible via a first interconnect;
 - at least two components of the integrated circuit, the components communicatively connected via a second interconnect; and
 - a memory suitable for storing a program of instructions, wherein the program of instructions configures the processor to optimize the integrated circuit based on heuristic data indicating past utilization of components of the integrated circuit, wherein the heuristic data is optimized based on at least one of bandwidth, latency, scalability, and isochronous interconnect configuration.
11. The self-programmable integrated circuit as described in claim 10, wherein the components include at least one of a core, functional block and logical block.
12. The self-programmable integrated circuit as described in claim 10, wherein the heuristic data includes data indicating amount of data transferred between a first component and a second component over the second interconnect.

13. An integrated circuit design system, comprising:
 - an electronic data storage device including a database having data describing integrated circuit component characteristics, firm macros and soft macros, wherein the data is optimized based on at least one of bandwidth, latency, scalability, and isochronous interconnect configuration; and
 - an agent implemented by a processor, the agent suitable for providing a design environment on an information handling system in which the design environment enables a user to design an integrated circuit to arrive at integrated circuit design data, the agent suitable for optimizing the integrated circuit design data utilizing the database having data describing integrated circuit component characteristics, firm macros and soft macros.
14. The integrated circuit design system as described in claim 13, wherein firm macros include a design of a logic function for specifying how logic elements are interconnected and specifies physical pathways and wiring patterns between components.
15. The integrated circuit design system as described in claim 14, wherein soft macros include a design of a logic function that specifies how logic elements are interconnected, but not physical wiring pattern on the chip.
16. The integrated circuit design system as described in claim 15, wherein heuristic data is utilized to derive at least one of the firm macro and soft macro.
17. The integrated circuit design system as described in claim 15, wherein heuristic

data includes data from previous circuit designs.

18. The integrated circuit design system as described in claim 15, wherein heuristic data includes data derived from operation of a circuit.
19. The integrated circuit design system as described in claim 13, wherein optimizing includes partitioning based on cost considerations.
20. The integrated circuit design system as described in claim 13, wherein at least one of a single integrated circuit and multiple integrated circuit solution is provided.